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EXAMINER	
CURS, NATHAN M	
ART UNIT	**PAPER NUMBER**
2633	6

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,009	YANG ET AL.	
	Examiner	Art Unit	
	Nathan Curs	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 5, line 2, "loss-pass" should be "low-pass"; page 13, line 17, "(a)" should be "(a')"; page 13, line 18, "(a)" should be "(a')" when referring to figure 4B; page 14, line 1, "T" should be "T'" and "(a)" should be "(a')" when referring to figure 4B; page 14, line 2, "(b)" should be "(b')" and "(a)" should be "(a')"; page 14, line 3, "T/8" should be "T'/8", "(a)" should be "(a')", "(b)" should be "(b')", and "(c)" should be "(c')"; page 14, line 8, "(c)" should be "(c')".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-13, 16-25, 27-33, 36, 37, and 40 are rejected under 35 U.S.C. 102(a) as being anticipated by Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2)

Regarding claims 1 and 17, Mokhtari et al. disclose an apparatus and method, comprising: a fiber optic system including an electrical 3R function (page 508, col. 2, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes a converter to convert an input

optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit receiving the original electrical signal (fig. 5 and page 509, col. 2, paragraph 1), generating a first signal corresponding to the original electrical signal delayed by a predetermined quantity of time and generating a second signal corresponding to the original electrical signal not delayed (fig. 5), comparing the first and second signals and forming a third signal in dependence upon the comparing of the first and second signals (fig. 5), detecting a bit rate in dependence upon the third signal (page 508, col. 1, paragraph 4 and page 509, col. 2, paragraphs 3 and 4); a clock generator generating a reference clock signal in dependence upon the detected bit rate and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3).

Regarding claim 2, Mokhtari et al. disclose an apparatus corresponding to an optical receiver receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4).

Regarding claim 3, Mokhtari et al. disclose that the bit rate of the input optical signal corresponds to a transmission rate (page 508, paragraphs 1, 3 and 4).

Regarding claim 4, Mokhtari et al. disclose an amplifier amplifying the original electrical signal received from the converter (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1).

Regarding claim 5, Mokhtari et al. disclose that the amplifier outputs the amplified electrical signal to the identification unit (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1; and fig. 1, fig. 3 and fig. 5).

Regarding claims 6 and 31, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including electrical 3R regeneration (page 508, col. 1, paragraph 3 and 4, and col.

2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4).

Regarding claims 7 and 32, Mokhtari et al. disclose an identification unit corresponding to a bit rate identification unit (fig. 3 and 5, and page 509, col. 2, paragraph 1).

Regarding claims 8 and 18, Mokhtari et al. disclose that the comparing performed by the identification unit corresponds to the identification unit performing an exclusive-OR logic operation upon the first and second signals (fig. 5).

Regarding claim 9, Mokhtari et al. disclose that the forming of the third signal performed by the identification unit corresponds to the identification unit forming the third signal in dependence upon the exclusive-OR logic operation performed upon the first and second signals (fig. 5).

Regarding claims 10 and 33, Mokhtari et al. disclose a first unit delaying the original electrical signal and performing the exclusive-OR operation upon the first and second signals and forming the third signal (fig. 5); and a second unit filtering the third signal, detecting the bit rate in dependence upon a voltage level of the filtered third signal (fig. 6 and page 509, col. 2, paragraph 4).

Regarding claims 11 and 37, Mokhtari et al. disclose that the filtering corresponds to low-pass filtering (page 509, col. 2, paragraph 4).

Regarding claim 12, Mokhtari et al. disclose a unit corresponding to a bit rate identification signal generator (fig. 3 and fig. 6 and page 509, col. 2, paragraph 4), where the filter output inherently corresponds to a bit rate identification signal.

Regarding claim 13, Mokhtari et al. disclose a unit corresponding to a bit rate deriving unit (fig. 6 and page 509, col. 2, paragraph 4), where the unit including the bank of oscillators

inherently derives a bit rate by tuning the VCO to the bit rate, based on the output signal from the filter.

Regarding claims 16, 27, 29, 36 and 40, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators generating clocking signals of different frequencies and selectively operating the oscillators to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

Regarding claims 19 and 25, Mokhtari et al. disclose receiving an original signal corresponding to an input optical signal (page 508, col. 1, paragraphs 3 and 4; and col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); outputting two duplicate signals substantially equivalent to the electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); and delaying the primary signal by the predetermined quantity of time (fig. 5 and page 509, col. 2, paragraph 1), and outputting a delayed primary signal corresponding to the first signal (fig. 5).

Regarding claim 20, Mokhtari et al. disclose a 3R regenerator with optoelectric conversion at the signal input (page 508, col. 2, paragraph 4), and disclose the first, second and third signals (fig. 5), where these three signal are inherently electrical for a 3R regenerator with optoelectric conversion.

Regarding claim 21 and 24, Mokhtari et al. disclose a method corresponding to receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4, and col. 2, paragraph 3).

Regarding claims 22 and 30, Mokhtari et al. disclose an original signal received corresponding to a plurality of original signals received (page 508, col. 1, paragraphs 3, 4, and

6), the recovering of the input clock signal and data from the original signal being performed for the plurality of original signals received (fig. 3 and page 509, col. 1, paragraphs 3 and 4), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4, and 6).

Regarding claim 23, Mokhtari et al. disclose recovering of the input clock signal and data from the original signal performed for a plurality of original signals received (fig. 2, fig. 3, page 509, col. 1, paragraphs 3, 4, and 5), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4 and 6).

Regarding claim 28, Mokhtari et al. disclose a 3R regenerator receiving an input optical signal (page 508, col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit receiving the original electrical signal (fig. 5 and page 509, col. 2, paragraph 1), generating a first signal corresponding to the original electrical signal delayed by a predetermine quantity of time and generating a second signal corresponding to the original electrical signal not delayed (fig. 5), forming a third signal by performing an exclusive-OR logic operation upon the first and second signals (fig. 5), detecting a bit rate in dependence upon the third signal and a clock generator generating a reference clock signal in dependence upon the detected bit rate (fig. 3, fig. 6 and page 509, col. 2, paragraphs 3 and 4); and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 15, 26, 35 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claims 15, 35 and 39, Mokhtari et al. disclose two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); a delay unit receiving the primary signal, delaying the primary signal by the predetermined quantity of time, outputting the primary signal, the delayed primary signal corresponding to the first signal (fig. 5); and an operator unit performing the exclusive-OR logic operation upon the first and second signals (fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit receiving the original electrical signal and outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., at the input of the Mokhtari et al. regenerator, to amplify the input signal and then output two duplicate signals directly to the compare circuit.

Regarding claim 26, Mokhtari et al. disclose a method, as described above, comprising: receiving an optical signal original signal using an optoelectric converter, converting the optic

signal to an electrical signal, forming two duplicate signals and delaying one of the signals by a predetermined quantity of time. Mokhtari et al. do not disclose that the two duplicate signals are output from a buffer. Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., at the input of the Mokhtari et al. regenerator, to amplify the input signal and then output two duplicate signals directly to the compare circuit.

6. Claims 14, 34, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Uda et al. (European Patent Office Publication No. 0342010) in view of Ishihara (US Patent No. 5557648).

Regarding claims 14, 34 and 38, Mokhtari et al. disclose a second unit comprising: a filter for filtering the signal output from the compare circuit, and determiner determining the bit rate in dependence upon the signal received from the filter (fig. 6; and page 509, col. 2, paragraph 4). Mokhtari et al. also disclose that the filter and determining circuits that follow the compare circuit (fig. 3) are part of a phase-locked loop, but do not disclose an analog-to-digital converter. Ishihara discloses a phase lock loop including a determining circuit that has an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the phase locked loop of Mokhtari et al., to digitize the filter output.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-38 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28, 29, 34, and 36-40 of copending Application No. 09/484061 in view of Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2).

Regarding claim 1 and 17, Application No. 09/484061 discloses an original electrical signal (claim 28, lines 3-7; and claim 38, lines 3-7) where the signal is inherently an electrical signal when it is compared to a delayed version of itself to produce a direct current voltage signal; an identification unit receiving the original electrical signal, and generating a first signal corresponding to the original electrical signal delayed by a predetermined quantity of time, generating a second signal corresponding to the original electrical signal not delayed, comparing the first and second signals, and forming a third signal in dependence upon the comparing of the first and second signals (claim 28, lines 3-5; and claim 38, lines 3-5), detecting a bit rate in dependence upon the third signal (claim 28, lines 6-7; and claim 38, lines 6-7).

Application No. 09/484061 does not disclose a converter converting an input optical signal to an electrical signal, but does disclose that the comparison signal is electrical (claim 28, line 6-7; and claim 38, lines 6-7) and that the original signal is received in wavelength division multiplexing transfer (claim 28, lines 1-2; and claim 38, lines 1-2). It would have been obvious to an artisan at the time of the invention that an electrical signal would be produced from the inherently optical WDM input signal using an optoelectric converter. Application No. 09/484061 does not disclose a clock generator generating a reference clock signal in dependence upon the detected bit rate or a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal. Mokhtari et al. disclose a bit-rate transparent regenerator (page 508, col. 1, paragraphs 3 and 4), with generation of a reference clock dependent on the detected bit rate and recovery of a data signal (fig. 2), including a comparing circuit that compares a signal with a delayed version of the same signal (fig. 3, fig. 5, and fig. 6). It would have been obvious to an artisan at the time of the invention to add a reference clock generator and recovery unit, as disclosed by Mokhtari et al., to the bit rate identifier disclosed in Application No. 09/484061, using the output of the bit rate identifier to generate the reference clock signal for the recovery unit, so that the original input signal can be regenerated independent of its bit-rate.

Regarding claim 2, 21, and 24, Application No. 09/484061 discloses receiving a WDM original signal (claim 28, lines 1-2), where a WDM signal is inherently optical, and determining the bit rate of the original signal according to a range corresponding to the measured voltage level (claim 36, lines 3-4), where a range of voltage levels representing the original signal bit rate inherently corresponds to receiving an original signal having a plurality of different bit rates.

Regarding claim 3, Application No. 09/484061 discloses identifying the bit rate of the input optical signal (claim 28, lines 6-7), where the bit rate of the input signal is inherently a transmission rate.

Regarding claims 4 and 5, Application No. 09/484061 does not disclose an amplifier amplifying the original electrical signal and outputting the signal to the identification unit. Mokhtari et al. disclose an amplifier amplifying an original electrical signal received from a converter and outputting the signal to an identification unit (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1; and fig. 1, fig. 3 and fig. 5). It would have been obvious to an artisan at the time of the invention to add an amplifier at the input after the converter and before the identification unit disclosed in Application No. 09/484061 to amplify the original signal for achieving an optimal signal level.

Regarding claims 6 and 31, Application No. 09/484061 discloses that the comparison signal is electrical (claim 28, line 6-7; and claim 38, lines 6-7) and that the original signal is received in a wavelength division multiplexing transfer (claim 28, lines 1-2; and claim 38, lines 1-2). It would have been obvious to an artisan at the time of the invention that the electrical signal would be produced from the inherently optical WDM input signal using an optoelectric converter.

Regarding claims 7 and 32, Application No. 09/484061 discloses an identification unit corresponding to a bit rate identification unit (claim 29, lines 5-6; and claim 39, lines 6-8).

Regarding claims 8 and 18, Application No. 09/484061 discloses that the comparing performed by the identification unit corresponds to the identification unit performing an exclusive-OR logic operation upon the first and second signals (claim 29, lines 5-6; and claim 39, lines 6-8).

Regarding claim 9, Application No. 09/484061 discloses that the forming of the third signal performed by the identification unit corresponds to the identification unit forming the third

signal in dependence upon the exclusive-OR logic operation performed upon the first and second signals (claim 29, lines 5-6; and claim 39, lines 6-8), where the selection signal is the third signal.

Regarding claims 10 and 33, Application No. 09/484061 discloses a first unit delaying the original electrical signal (claim 28, lines 3-5; and claim 38, lines 3-5) and performing the exclusive-OR operation upon the first and second signals and forming the third signal (claim 29, lines 5-6; and claim 39, lines 6-8); and detecting the bit rate in dependence upon a direct current voltage level of the third signal (claim 28, lines 6-7; and claim 38, lines 6-7); where a filter unit is inherently used to create a direct current voltage signal from the bit rate identification signal.

Regarding claims 11 and 37, Application No. 09/484061 discloses determining the bit rate based on the direct voltage level of the selection signal (claim 28, lines 6-7), where a low pass filter is inherently required to create a direct current voltage signal from the bit rate selection signal.

Regarding claim 12, Application No. 09/484061 discloses a first unit corresponding to a bit rate identification signal generator (claim 28, lines 3-5 and claim 29, lines 5-6).

Regarding claim 13, Application No. 09/484061 discloses a second unit corresponding to a bit rate deriving unit (claim 28, lines 6-7).

Regarding claims 14, 34 and 38, Application No. 09/484061 discloses a second unit comprising: a filter for filtering the signal output from the compare circuit (claim 34, lines 1-2; and claim 40, line 2), a determiner determining the bit rate in dependence upon the signal received from the filter (claim 36, lines 2-4; and claim 40, lines 3-4), and an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (claim 37, lines 1-2).

Regarding claim 15, Application No. 09/484061 discloses a buffer unit receiving the original electrical signal and outputting two duplicate signals substantially equivalent to the original electrical signal (claim 39, lines 2-3), the two duplicate signals corresponding to a primary signal and a secondary signal, and a delay unit receiving the primary signal, delaying the primary signal by the predetermined quantity of time, outputting the primary signal, the delayed primary signal corresponding to the first signal (claim 28, lines 3-5; and claim 38, lines 3-5); and an operator unit performing the exclusive-OR logic operation upon the first and second signals (claim 29, lines 4-6; and claim 39, lines 6-8).

Regarding claims 16, 27, 29 and 36, Application No. 09/484061 does not disclose a clock generator. Mokhtari et al. disclose a clock generator and clock generation method comprising a plurality of oscillators generating clocking signals of different frequencies and Mokhtari et al. also discloses selectively operating the oscillators to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4). It would have been obvious to an artisan at the time of the invention to add a reference clock generator comprising selection among a plurality of oscillators, as disclosed by Mokhtari et al., to the bit rate identifier disclosed in Application No. 09/484061, using the output of the bit rate identifier to generate the reference clock signal at the frequency corresponding to the bit rate, so that the original input signal can be regenerated independent of its bit-rate.

Regarding claims 19 and 25, Application No. 09/484061 discloses receiving an original signal corresponding to an input optical signal, converting the input optical signal to an electrical signal, as described above, and outputting two duplicate signals substantially equivalent to the electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal, delaying the primary signal by the predetermined quantity of time, and outputting a delayed primary signal corresponding to the first signal (claim 28, lines 3-5).

Regarding claim 20, Application No. 09/484061 discloses first, second and third signals (claim 28, lines 3-6), where the signals are inherently electrical if a direct current voltage is measured from the third signal, which is a result of comparison of the first and second signals.

Regarding claims 22, 23 and 30, Application No. 09/484061 discloses determining the bit rate of the original signal according to a range corresponding to the measured voltage level (claim 36, lines 3-4), where a range of voltage levels representing the original signal bit rate inherently corresponds to receiving an original signal having a plurality of different bit rates. Application No. 09/484061 does not disclose a clock generator generating a reference clock signal in dependence upon the detected bit rate and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal. Mokhtari et al. disclose a bit-rate transparent regenerator (page 508, col. 1, paragraphs 3 and 4), with generation of a reference clock dependent on the detected bit rate and recovery of a data signal (fig. 2), including a comparing circuit that compares a signal with a delayed version of the same signal (fig. 3, fig. 5, and fig. 6). It would have been obvious to an artisan at the time of the invention to add a reference clock generator and recovery unit, as disclosed by Mokhtari et al., to the bit rate identifier disclosed in Application No. 09/484061, using the output of the bit rate identifier to generate the reference clock signal for the recovery unit, so that the original input signal can be regenerated independent of its bit-rate.

Regarding claim 26, Application No. 09/484061 discloses receiving an optical original signal (claim 28, lines 1-2; and claim 38, lines 1-2), where a WDM signal is inherently optical; forming two duplicate signals based on the original signal and delaying one of the signals by a predetermined quantity of time (claim 28, lines 3-5; and claim 38, lines 3-5), where the outputting of the two duplicate signals is performed by a buffer (claim 39, lines 2-3). Application No. 09/484061 also discloses generating a selection signal based on a comparison of the

original and delayed signals and extracting the bit rate of the original signal by measuring a voltage level of the selection signal (claim 28, lines 3-7; and claim 38, lines 3-7), where an optoelectric converter is inherently used to convert an optical input signal to an electrical signal before the electrical signal is duplicated and compared to a delayed version of itself to produce a direct current voltage signal.

Regarding claim 28, Application No. 09/484061 discloses an input optical signal (claim 28, lines 1-2; and claim 38, lines 1-2), where a WDM signal is inherently optical; an identification unit receiving a signal and generating a first signal corresponding to the signal delayed by a predetermine quantity of time, generating a second signal corresponding to the signal not delayed, forming a third signal by performing an exclusive-OR logic operation upon the first and second signals (claim 28, lines 3-5 and claim 29, lines 2-6; and claim 38, lines 3-5 and claim 39, lines 6-8), and detecting a bit rate in dependence upon the third signal (claim 28, lines 6-7; and claim 38, lines 6-7). Application No. 09/484061 also discloses detecting the bit rate by measuring a voltage level of the third signal (claim 28, lines 6-7; and claim 38, lines 6-7), where an optoelectric converter is inherently required to convert an optical input signal to an electrical signal before the electrical signal is duplicated and compared to a delayed version of itself to produce a direct current voltage signal. Application No. 09/484061 does not disclose a clock generator generating a reference clock signal in dependence upon the detected bit rate and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal. Mokhtari et al. disclose a bit-rate transparent regenerator (page 508, col. 1, paragraphs 3 and 4), with generation of a reference clock dependent on the detected bit rate and recovery of a data signal (fig. 2), including a comparing circuit that compares a signal with a delayed version of the same signal (fig. 3, fig. 5, and fig. 6). It would have been obvious to an artisan at the time of the invention to add a reference clock

generator and recovery unit, as disclosed by Mokhtari et al., to the bit rate identifier disclosed in Application No. 09/484061, using the output of the bit rate identifier to generate the reference clock signal for the recovery unit, so that the original input signal can be regenerated independent of its bit-rate.

This is a provisional obviousness-type double patenting rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- US Patent No. 4361897 – Note a clock recovery circuit where an XOR circuit receives two signals that are duplicates of an input signal, where one of the duplicates is delayed prior to entering the XOR circuit (fig. 1, element E; and col. 2, lines 12-22).

10. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (703) 305-0370. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

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